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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/619,521 | 07/14/2003 | Qing Deng | 10003809-7 | 7465 |

7590 04/06/2005

AGILENT TECHNOLOGIES, INC.
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| EXAMINER | |
|---|---|
| VAN ROY, TOD THOMAS | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2828 | |

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H-B

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/619,521 | DENG ET AL. | |
| | Examiner | Art Unit | |
| | Tod T. Van Roy | 2828 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 47-60 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 47-60 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 10/17/2003.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 47, and 54 are rejected under 35 U.S.C. 102(b) as being anticipated by Ramdani et al. (US 5835521).

With respect to claim 47, Ramdani discloses a VCSEL (fig.3) comprising a first mirror stack (fig.3 #13), a second mirror stack (fig.3 #42) a cavity region disposed between the first mirror stack and the second mirror stack (fig.3 #34) and including an active region, a defect source (col.5 lines 45-52, emphasis on lines 50-52), and a reliability-enhancing layer positioned within the defect source to reduce defect induced degradation of one or more VCSEL regions (fig.3 #31, col.5 lines 9-10).

With respect to claim 54, Ramdani discloses a method of manufacturing a VCSEL comprising forming a first mirror stack (col.3 lines 26-33), a second mirror stack (col.6 lines 4-6) a cavity region disposed between the first mirror stack and the second mirror stack (col.5 lines 11-13) and including an active region, a defect source (col.5 lines 45-52, emphasis on lines 50-52), and a reliability-enhancing layer positioned within the defect source to reduce defect induced degradation of one or more VCSEL regions (col.5 lines 9-10).

Claims 48-51, 53, 55-58, and 60 are rejected under 35 U.S.C. 102(b) as being anticipated by Yuen et al. (US 5991326).

With respect to claim 48, Yuen discloses the claimed VCSEL (fig.1) comprising a first mirror stack (fig.1 #10), a second mirror stack (fig.1 #32), a cavity region disposed between the first mirror stack and the second mirror stack (fig.1 #16) including an active region (fig.1 #20), a defect source (fig.3 #46), and a reliability-enhancing layer (fig.1 #32 bottom layer, when material of type InGaAsP, col.5 lines 20-21) positioned with respect to the defect source to reduce defect induced degradation of one or more VCSEL regions, where the defect source is disposed between the reliability-enhancing layer and the cavity region (fig.3, oxidized region between InGaAsP mirror layer and cavity region)

With respect to claim 49, Yuen discloses the VCSEL as described above, further comprising a second reliability-enhancing layer separated from the first reliability-enhancing layer by one or more other layers (fig.1 #18, col.4 lines 19-21), wherein the first and second reliability-enhancing layers are located on opposite sides of the defect source (bottom layer of DBR 32 on top of defect oxide region while spacer 18 below the defect region).

With respect to claims 50 and 51, Yuen discloses the claimed VCSEL (fig.1) comprising a first mirror stack (fig.1 #10), a second mirror stack (fig.1 #32), a cavity region disposed between the first mirror stack and the second mirror stack (fig.1 #16) including an active region (fig.1 #20), a defect source (fig.3 #46), and a reliability-enhancing layer (fig.1 #26, col.4 lines 51-53) positioned with respect to the defect

source to reduce defect induced degradation of one or more VCSEL regions, wherein the reliability-enhancing layer is configured to at least in part balance strain created by the defect source (layer 26 is used to prevent lattice mismatch with the quantum well, col.4 lines 54-56, and is located within the strain field of the defect region 46 and inherently performs the strain balancing function because it has the same structure and composition as the instant invention).

With respect to claim 53, Yuen discloses the claimed VCSEL (fig.1) comprising a first mirror stack (fig.1 #10), a second mirror stack (fig.1 #32), a cavity region disposed between the first mirror stack and the second mirror stack (fig.1 #16) including an active region (fig.1 #20), a defect source (fig.3 #46), and a reliability-enhancing layer (fig.1 #26, col.4 lines 51-53) positioned with respect to the defect source to reduce defect induced degradation of one or more VCSEL regions, wherein the defect source creates a concentration gradient inducing defect migration, and the reliability-enhancing layer is configured to reduce the induced defect migration (layer 26 inherently reduces defect migration because it has the same structure and composition as the instant invention).

With respect to claim 55, Yuen discloses a method of manufacturing a VCSEL comprising forming a first mirror stack, a second mirror stack, and a cavity region disposed there between, wherein the cavity region includes an active region (col.5 lines 43-49), forming a defect source (col.4 lines 66-67), forming a reliability-enhancing layer (fig.1 #32 bottom layer, when material of type InGaAsP, col.5 lines 20-21) positioned with respect to the defect source to reduce defect induced degradation of one or more VCSEL regions, where the defect source is disposed between the reliability-enhancing

layer and the cavity region (fig.3, oxidized region between InGaAsP mirror layer and cavity region).

With respect to claim 56, Yuen discloses the method outlined in rejection to claim 55 further comprising forming a second reliability-enhancing layer separated from the first reliability-enhancing layer by one or more other layers (fig.1 #18, col.4 lines 19-21), wherein the first and second reliability-enhancing layers are located on opposite sides of the defect source (bottom layer of DBR 32 on top of defect oxide region while spacer 18 below the defect region).

With respect to claims 57 and 58, Yuen discloses a method of manufacturing a VCSEL comprising forming a first mirror stack, a second mirror stack, and a cavity region disposed there between, wherein the cavity region includes an active region (col.5 lines 43-49), forming a defect source (col.4 lines 66-67), forming a reliability-enhancing layer (fig.1 #26 col.4 lines 51-53) positioned with respect to the defect source to reduce defect induced degradation of one or more VCSEL regions, wherein the reliability-enhancing layer is configured to at least in part balance strain created by the defect source (layer 26 is used to prevent lattice mismatch with the quantum well, col.4 lines 54-56, and is located within the strain field of the defect region 46 and inherently performs the strain balancing function because it has the same structure and composition as the instant invention).

With respect to claim 60, Yuen discloses a method of manufacturing a VCSEL comprising forming a first mirror stack, a second mirror stack, and a cavity region disposed there between, wherein the cavity region includes an active region (col.5 lines

43-49), forming a defect source (col.4 lines 66-67), forming a reliability-enhancing layer (fig.1 #26 col.4 lines 51-53) positioned with respect to the defect source to reduce defect induced degradation of one or more VCSEL regions, wherein the defect source creates a concentration gradient inducing defect migration, and the reliability-enhancing layer is configured to reduce the induced defect migration (layer 26 inherently reduces defect migration because it has the same structure and composition as the instant invention).

Claims 50, and 57 are rejected under 35 U.S.C. 102(b) as being anticipated by Duggan (US 5991321).

With respect to claim 50, Duggan discloses the claimed VCSEL (fig.13) comprising a first mirror stack (fig.13 #28), a second mirror stack (fig.13 #26), a cavity region disposed between the first mirror stack and the second mirror stack (fig.13 #12) including an active region (fig.13 #10), a defect source (fig.13 #30), and a reliability-enhancing layer (fig.13 #6, col.8 lines 14-15) positioned with respect to the defect source to reduce defect induced degradation of one or more VCSEL regions, wherein the reliability-enhancing layer is configured to at least in part balance strain created by the defect source (layer 6 is located within the strain field of the defect region 30 and inherently performs the strain balancing function because it has the same structure and composition as the instant invention).

With respect to claim 57, Duggan discloses a method of manufacturing a VCSEL comprising forming a first mirror stack, a second mirror stack (col.8 lines 44-45), and a

cavity region disposed there between, wherein the cavity region includes an active region (col.8 lines 34-38), forming a defect source (col.8 lines 45-47), forming a reliability-enhancing layer (fig.13 #6, col.8 lines 14-15) positioned with respect to the defect source to reduce defect induced degradation of one or more VCSEL regions, wherein the reliability-enhancing layer is configured to at least in part balance strain created by the defect source (layer 26 is used to prevent lattice mismatch with the quantum well, col.4 lines 54-56, and is located within the strain field of the defect region 46 and inherently performs the strain balancing function because it has the same structure and composition as the instant invention).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 52 and 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Duggan in view of Yuen.

With respect to claim 52, Dugan teaches the VCSEL outlined in rejection of claim 50 above, comprising the reliability-enhancing layer formed of InxGa1-xP wherein x<0.5 (col.7 lines 13-17), Dugan does not teach one of the first and second mirror stacks to comprise oxidized AlGaAs layers. Yuen teaches DBR layers to be made of oxidized AlGaAs (col.5 lines 20-25). It would have been obvious at the time of the invention to one of ordinary skill in the art to combine the VCSEL of Dugan with the oxidized AlGaAs mirror stack of Yuen to provide a large refractive index difference between the adjacent DBR layers and increase the DBR stop bandwidth and relax the growth accuracy for the DBR (Yuen, col.5 lines 25-32).

With respect to claim 59, Dugan teaches the method of forming the VCSEL as outlined in the rejection of claim 57 above, comprising the reliability-enhancing layer formed of InxGa1-xP wherein x<0.5 (col.7 lines 13-17), Dugan does not teach one of the first and second mirror stacks to be formed of oxidized AlGaAs layers. Yuen teaches DBR layers to be formed of oxidized AlGaAs (col.5 lines 13, 20-25). It would have been obvious at the time of the invention to one of ordinary skill in the art to combine the VCSEL formation method of Dugan with the oxidized AlGaAs mirror stack formation of Yuen to provide a large refractive index difference between the adjacent DBR layers and increase the DBR stop bandwidth and relax the growth accuracy for the DBR (Yuen, col.5 lines 25-32).

### *Double Patenting*

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 47-60 rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-3, 6, 16-19, 29-30, 34, and 43-46 of U.S. Patent No. 6628694. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claims in the current application are broader than the claims of patent '694 and hence '694 then outlines an existing embodiment of the claims of the application under review.

### *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tod T. Van Roy whose telephone number is (571)272-8447. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Minsun Harvey can be reached on (571)272-1835. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVR